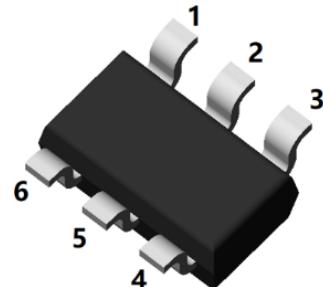
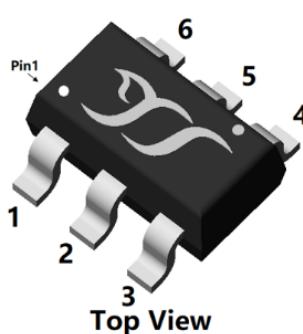
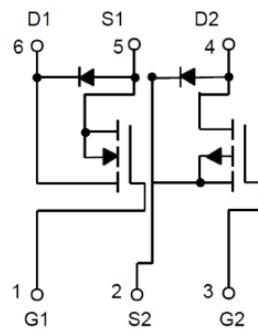


## N-Channel and P-Channel Complementary Power MOSFET


**SOT-23-6L**


### Product Summary

#### NMOS(Die1)

- $V_{DS}$  20V
- $I_D$  2.0A
- $R_{DS(ON)}$  ( at  $V_{GS}=4.5V$ ) <55 mohm
- $R_{DS(ON)}$  ( at  $V_{GS}=2.5V$ ) <75 mohm

#### PMOS(Die2)

- $V_{DS}$  -20V
- $I_D$  -1.5A
- $R_{DS(ON)}$  ( at  $V_{GS}=-4.5V$ ) <120 mohm
- $R_{DS(ON)}$  ( at  $V_{GS}=-2.5V$ ) <170 mohm

### General Description

- Trench Power LV MOSFET technology
- High Density Cell Design for Low  $R_{DS(ON)}$
- High Speed switching
- Part no. with suffix "Q" means AEC-Q101 qualified

### Applications

- Interfacing, Logic switch
- Load switch
- Power management

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-source Voltage		$V_{DS}$	20	-20	V
Gate-source Voltage		$V_{GS}$	$\pm 10$	$\pm 10$	V
Drain Current	$T_A=25^\circ\text{C}$	$I_D$	2.0	-1.5	A
	$T_A=100^\circ\text{C}$		1.3	-1.0	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	12	-12	A
Total Power Dissipation <sup>B</sup>	$T_A=25^\circ\text{C}$	$P_D$	595	568	mW
	$T_A=100^\circ\text{C}$		238	227	mW
Thermal Resistance Junction-to-Case @ Steady State <sup>C</sup>		$R_{\theta JA}$	210	220	$^\circ\text{C} / \text{W}$
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	-55~+150	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJJ2429AQ	F2	2429	3000	30000	120000	7" reel

■ N-MOS Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	20			V
Zero Gate Voltage Drain Current	$I_{\text{DS}}^{\text{SS}}$	$V_{\text{DS}}=20\text{V}, V_{\text{GS}}=0\text{V}$			1	$\mu\text{A}$
Gate-Body Leakage Current	$I_{\text{GSS}}$	$V_{\text{GS}}= \pm 10\text{V}, V_{\text{DS}}=0\text{V}$			$\pm 100$	nA
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	0.5	0.75	1.1	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}= 4.5\text{V}, I_{\text{D}}=1\text{A}$		38	55	$\text{m}\Omega$
		$V_{\text{GS}}= 2.5\text{V}, I_{\text{D}}=0.6\text{A}$		50	75	
Diode Forward Voltage <sup>C</sup>	$V_{\text{SD}}$	$I_{\text{S}}=1\text{A}, V_{\text{GS}}=0\text{V}$		0.85	1.2	V
Gate resistance	$R_{\text{G}}$	f=1MHz	-	2.5		$\Omega$
<b>Dynamic Parameters <sup>B</sup></b>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}}=10\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$		186		$\text{pF}$
Output Capacitance	$C_{\text{oss}}$			33		
Reverse Transfer Capacitance	$C_{\text{rss}}$			27		
<b>Switching Parameters <sup>B</sup></b>						
Total Gate Charge	$Q_{\text{g}}$	$V_{\text{GS}}=4.5\text{V}, V_{\text{DS}}=10\text{V}, I_{\text{D}}=2\text{A}$		3.2		$\text{nC}$
Gate Source Charge	$Q_{\text{gs}}$			0.8		
Gate Drain Charge	$Q_{\text{gd}}$			0.8		
Reverse Recovery Charge	$Q_{\text{rr}}$	$I_{\text{SD}}=2\text{A}, dI/dt=80\text{A/us}$		0.95		$\text{ns}$
Reverse Recovery Time	$t_{\text{rr}}$			4.9		
Turn-on Delay Time	$t_{\text{D(on)}}$			4.8		
Turn-on Rise Time	$t_{\text{r}}$	$V_{\text{GS}}=4.5\text{V}, V_{\text{DS}}=10\text{V}, I_{\text{D}}=2\text{A}, R_{\text{g}}=3\Omega$		28		$\text{ns}$
Turn-off Delay Time	$t_{\text{D(off)}}$			15		
Turn-off Fall Time	$t_{\text{f}}$			28		

- A. Repetitive rating; pulse width limited by max. junction temperature.  
B.  $P_d$  is based on max. junction temperature, using junction-case thermal resistance.  
C. The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in the still air environment with  $T_A=25^\circ\text{C}$ . The maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design.



## ■ P-MOS Electrical Characteristics (TJ=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =-250μA	-20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C			-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±10V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.3	-0.65	-1.0	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = -4.5V, I <sub>D</sub> =-1A		86	120	mΩ
		V <sub>GS</sub> = -2.5V, I <sub>D</sub> =-0.6A		115	170	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-0.5A, V <sub>GS</sub> =0V			-1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz	-	15	-	Ω
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V, f=1MHz		70		pF
Output Capacitance	C <sub>oss</sub>			19		
Reverse Transfer Capacitance	C <sub>rss</sub>			14		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-10V, I <sub>D</sub> =-1.2A		2.9		nC
Gate Source Charge	Q <sub>gs</sub>			0.65		
Gate Drain Charge	Q <sub>gd</sub>			0.7		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>SD</sub> =-1.2A, di/dt=60A/us		0.9		ns
Reverse Recovery Time	t <sub>rr</sub>			5.4		
Turn-on Delay Time	t <sub>D(on)</sub>			4.8		
Turn-on Rise Time	t <sub>r</sub>	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-10V, I <sub>D</sub> =-1.2A, R <sub>g</sub> =3Ω		22		ns
Turn-off Delay Time	t <sub>D(off)</sub>			21		
Turn-off Fall Time	t <sub>f</sub>			28		

## ■ N-MOS Typical Performance Characteristics

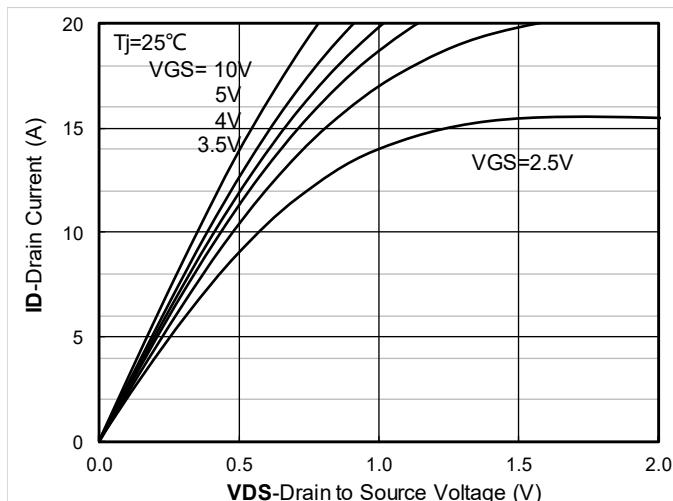


Figure1. Output Characteristics

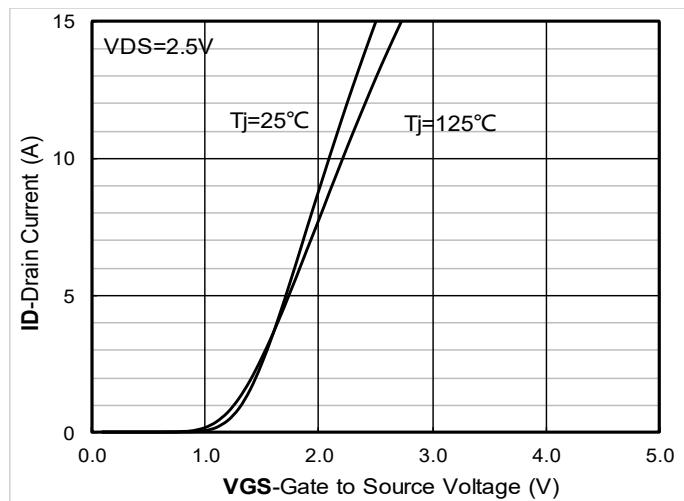


Figure2. Transfer Characteristics

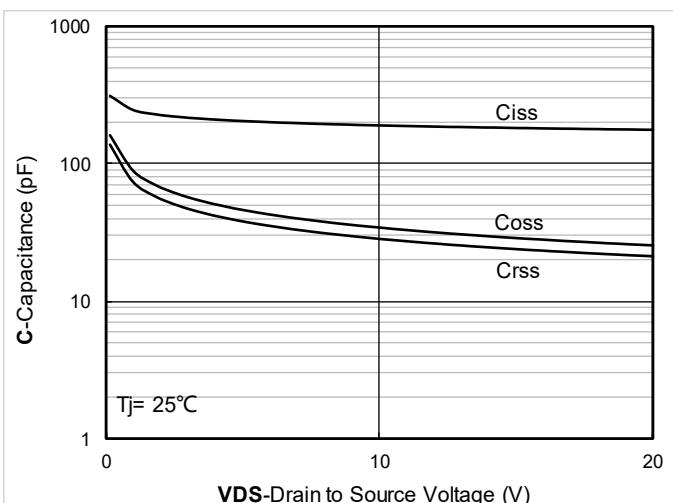


Figure3. Capacitance Characteristics

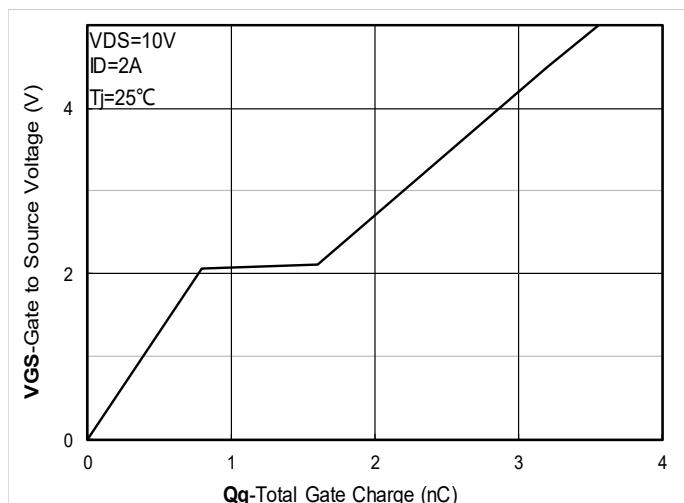


Figure4. Gate Charge

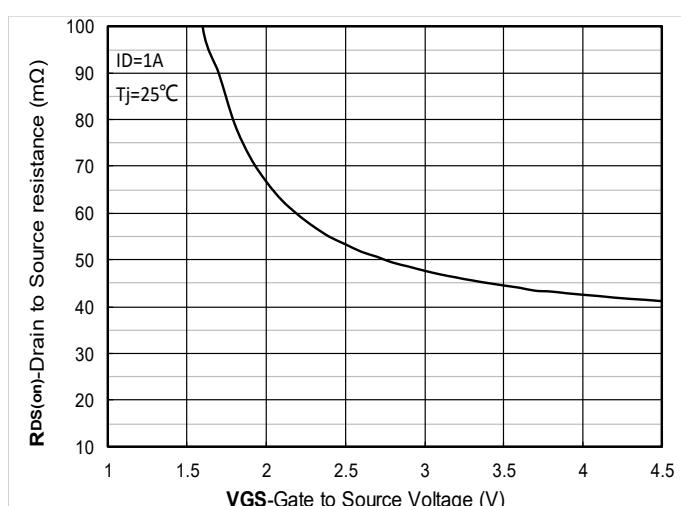


Figure5. On-Resistance vs Gate to Source Voltage

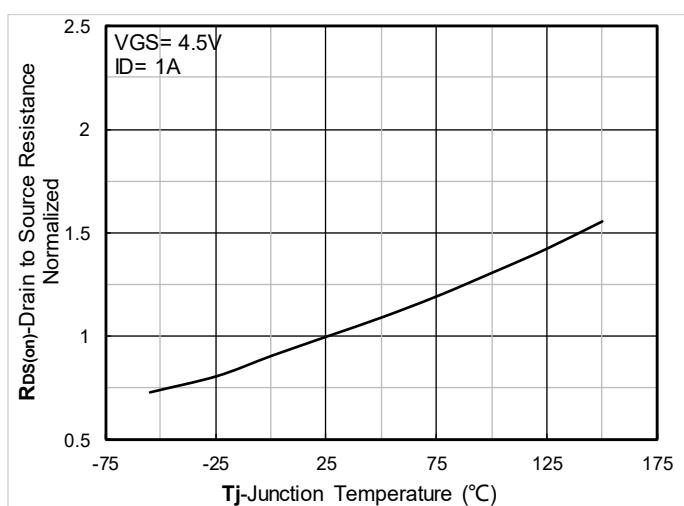
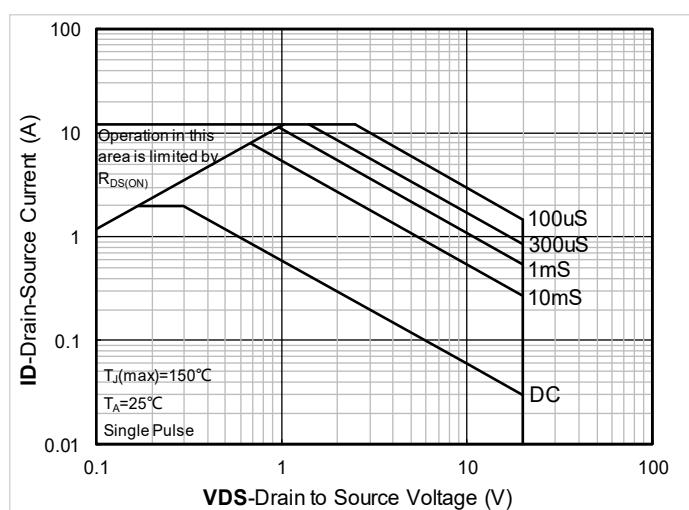
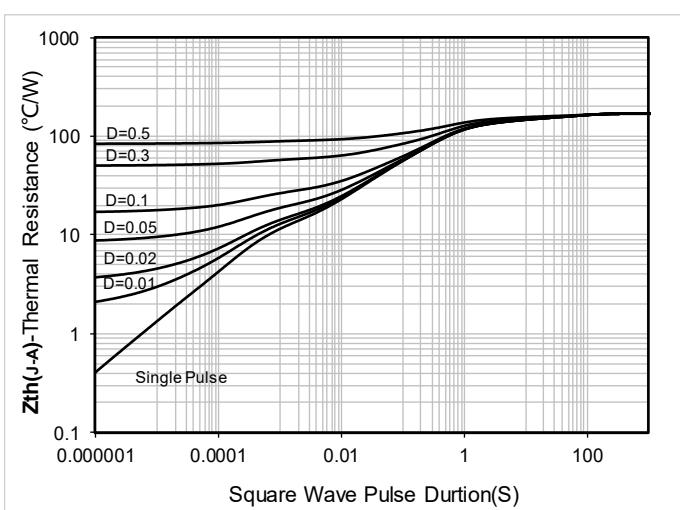
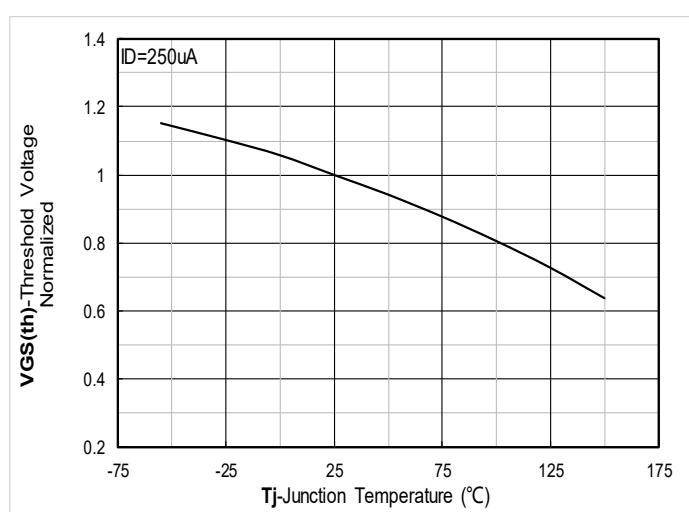
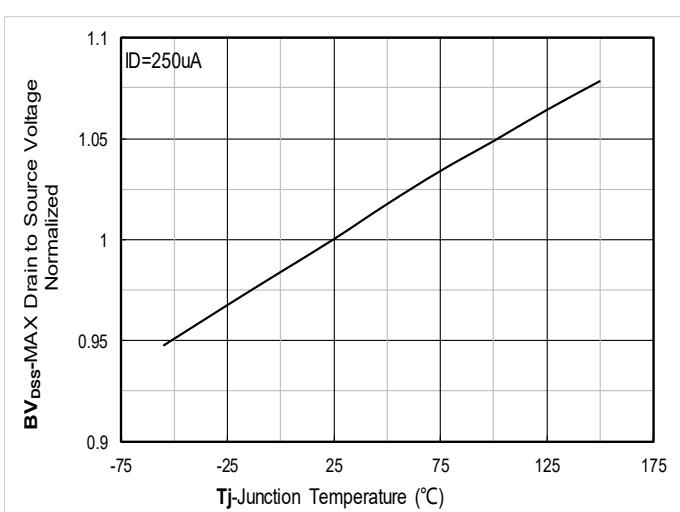
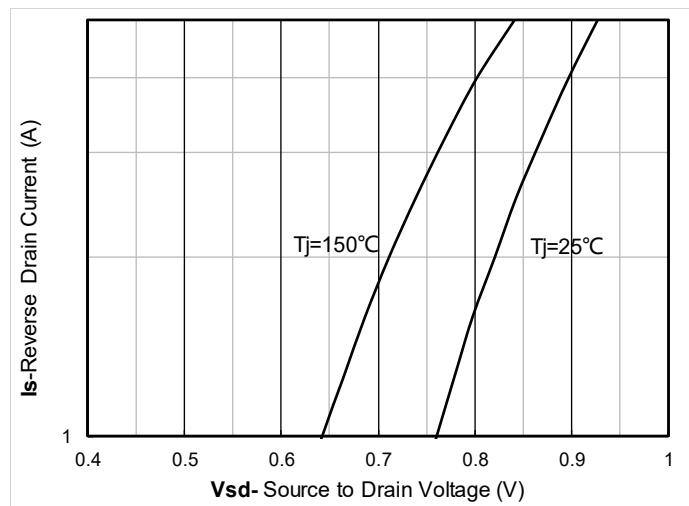
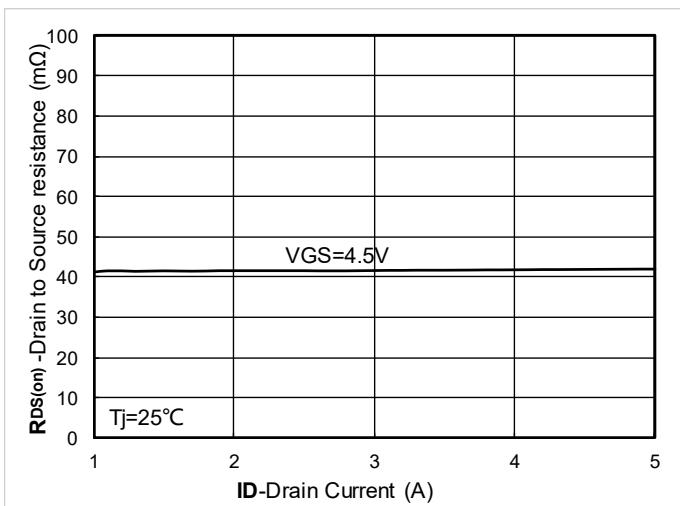


Figure6. Normalized On-Resistance



## ■ P-MOS Typical Performance Characteristics

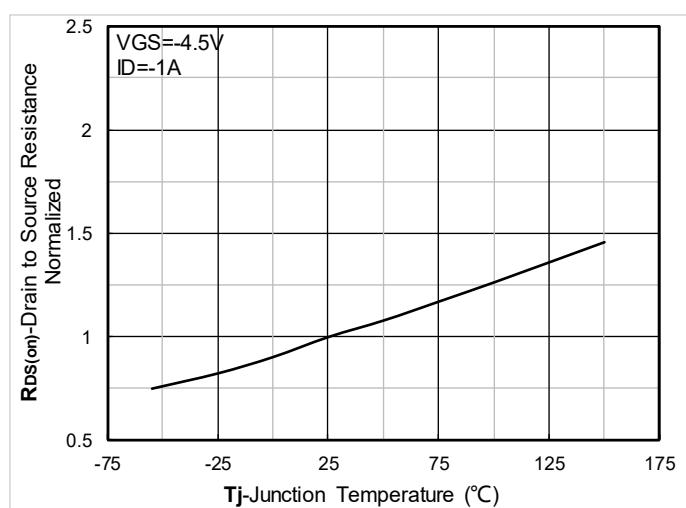
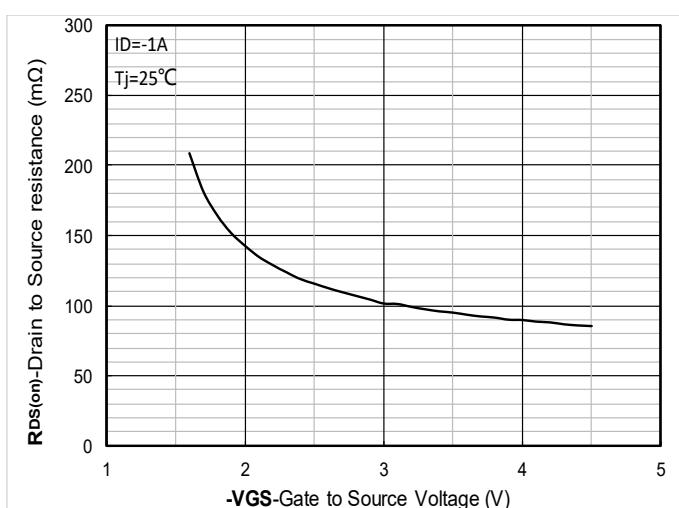
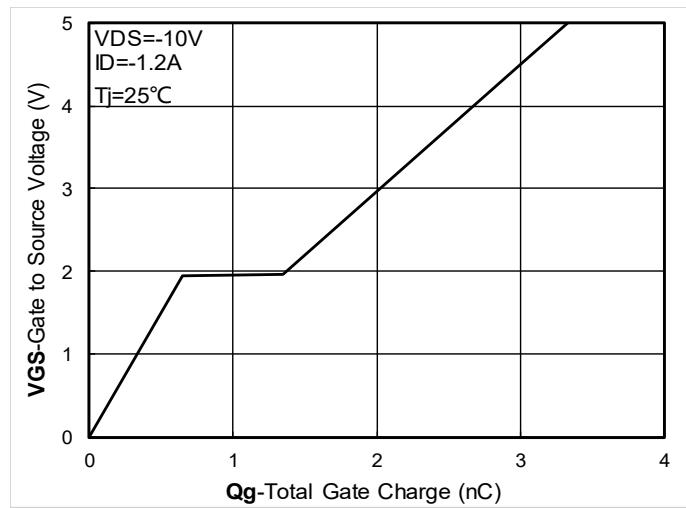
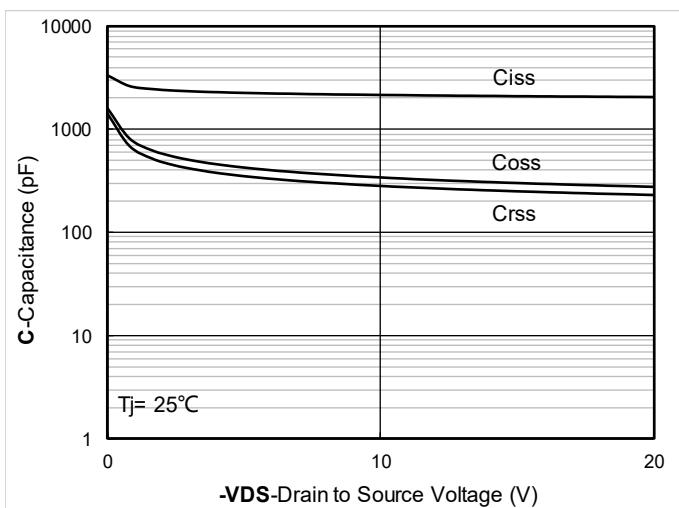
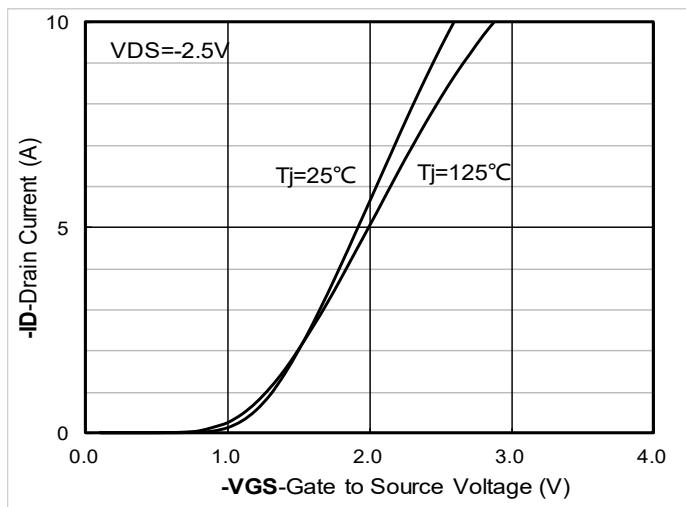
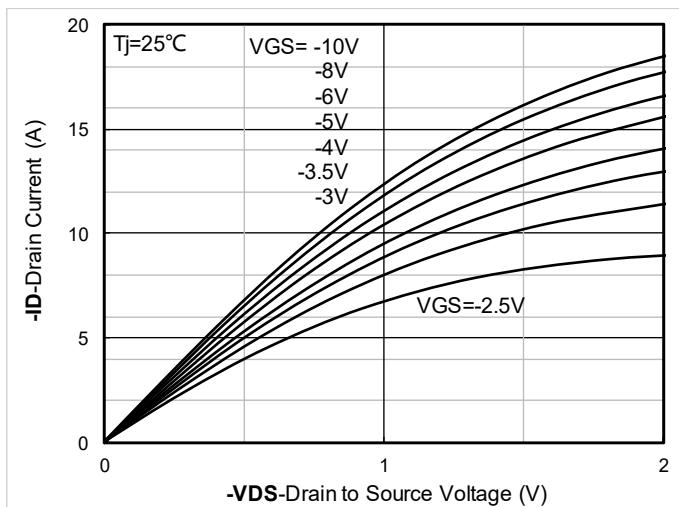


Figure 5. On-Resistance vs Gate to Source Voltage

Figure 6. Normalized On-Resistance

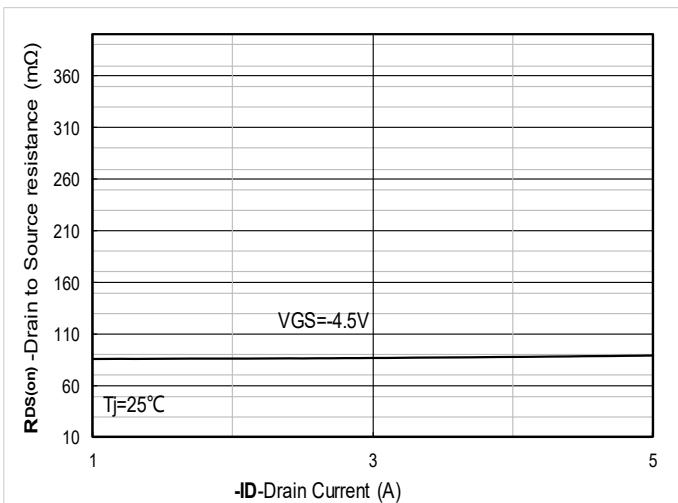


Figure 7.  $R_{DS(on)}$  VS Drain Current

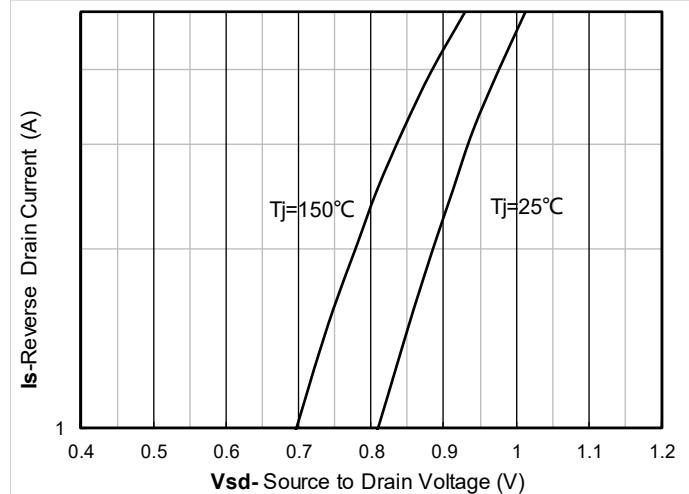


Figure 8. Forward characteristics of reverse diode

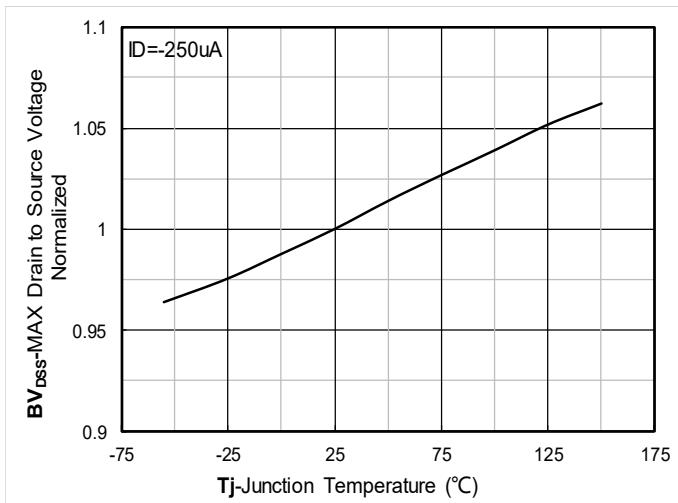


Figure 9. Normalized breakdown voltage

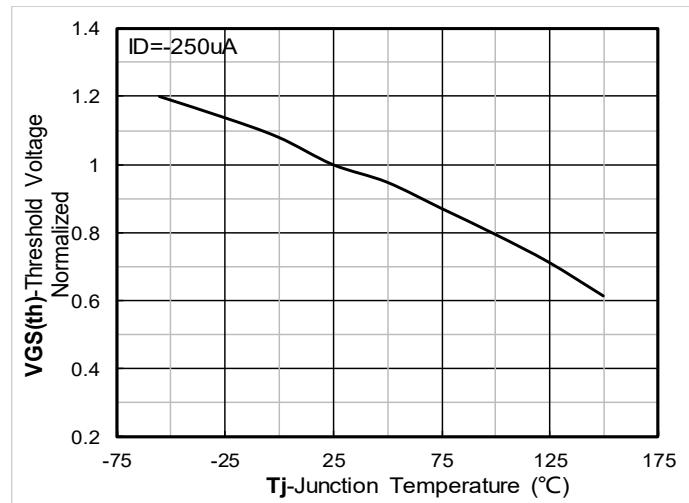


Figure 10. Normalized Threshold voltage

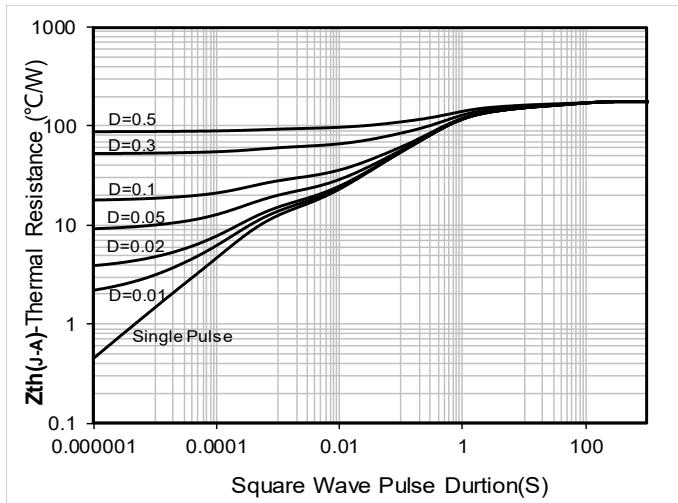


Figure 11. Maximum Transient Thermal Impedance

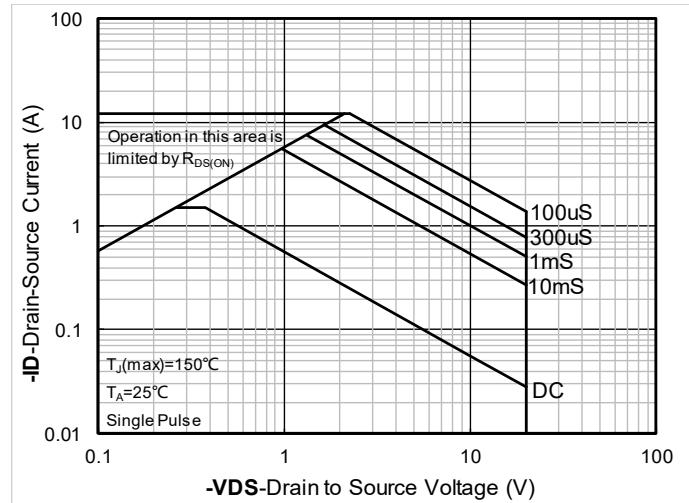
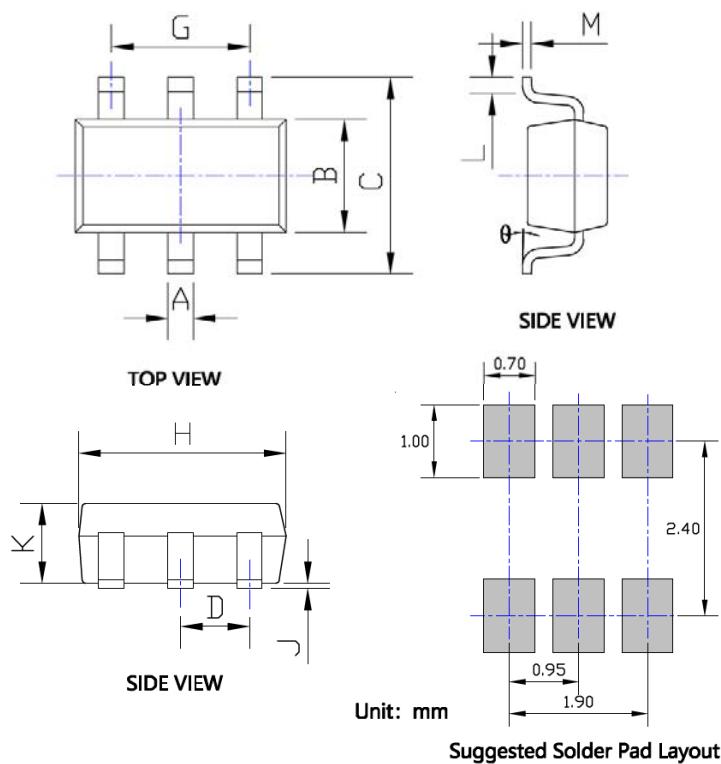


Figure 12. Safe Operation Area

**■ SOT-23-6L Package Information**

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.012	0.020	0.300	0.500
B	0.059	0.067	1.500	1.700
C	0.104	0.116	2.650	2.950
D	0.037BSC		0.950BSC	
G	0.075BSC		1.900BSC	
H	0.111	0.119	2.820	3.020
J	0.000	0.004	0.000	0.100
K	0.041	0.045	1.050	1.150
L	0.012	0.024	0.300	0.600
M	0.004	0.008	0.100	0.200
θ	0°	8°	0°	8°

**Note:**

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.05\text{mm}$ .
3. The pad layout is for reference purposes only.



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