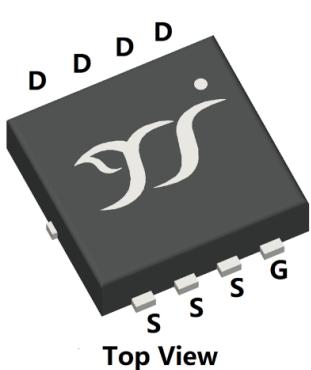
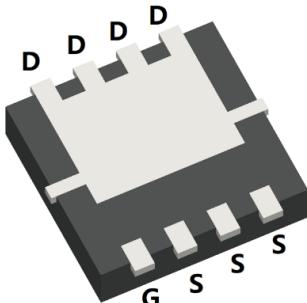
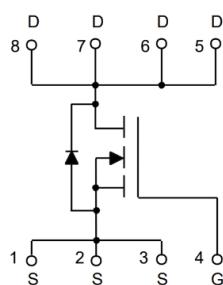


**N-Channel Enhancement Mode Field Effect Transistor**

Top View



Bottom View

PDFN3333-8L**■ Absolute Maximum Ratings (T_A=25°C unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V _{DS}	25	V
Gate-source Voltage	V _{GS}	±20	V
Drain Current	I _D	14	A
T _A =25°C		8.5	
T _A =100°C		60	
T _C =25°C		38	
Pulsed Drain Current ^A	I _{DM}	200	A
Avalanche energy ^B	EAS	78	mJ
Total Power Dissipation ^C	P _D	1.92	W
T _A =25°C		0.77	
T _A =100°C		50	
T _C =25°C		20	
Junction and Storage Temperature Range	T _J , T _{STG}	-55~+150	°C

■ Thermal resistance

Parameter	Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	R _{θJA}	55	65	°C/W
Thermal Resistance Junction-to-Case	R _{θJC}	2	2.5	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ60N025A	F1	Q60N025A	5000	10000	100000	13" reel



YJQ60N025A

■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	25	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=25\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
		$V_{\text{DS}}=25\text{V}, V_{\text{GS}}=0\text{V}, T_J=150^\circ\text{C}$	-	-	100	
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=30\text{A}$	-	3.5	4.6	$\text{m}\Omega$
		$V_{\text{GS}}=10\text{V}, I_{\text{D}}=16\text{A}$	-	3.5	4.6	
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=10\text{A}$	-	7.4	10	
Diode Forward Voltage	V_{SD}	$I_{\text{S}}=30\text{A}, V_{\text{GS}}=0\text{V}$	-	-	1.2	V
Gate resistance	R_{G}	$f=1\text{MHz}$	-	2	-	Ω
Maximum Body-Diode Continuous Current	I_{S}		-	-	60	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{DS}}=12.5\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	-	1035	-	pF
Output Capacitance	C_{oss}		-	225	-	
Reverse Transfer Capacitance	C_{rss}		-	195	-	
Switching Parameters						
Total Gate Charge	Q_{g}	$V_{\text{GS}}=10\text{V}, V_{\text{DS}}=12.5\text{V}, I_{\text{D}}=30\text{A}$	-	23	-	nC
Gate-Source Charge	Q_{gs}		-	5.2	-	
Gate-Drain Charge	Q_{gd}		-	5.7	-	
Reverse Recovery Charge	Q_{rr}	$I_{\text{F}}=30\text{A}, \text{di}/\text{dt}=100\text{A}/\text{us}$	-	0.35	-	nC
Reverse Recovery Time	t_{rr}		-	5.7	-	
Turn-on Delay Time	$t_{\text{D(on)}}$		-	6	-	
Turn-on Rise Time	t_{r}	$V_{\text{GS}}=10\text{V}, V_{\text{DD}}=12.5\text{V}, I_{\text{D}}=30\text{A}$ $R_{\text{GEN}}=3\Omega$	-	20.5	-	ns
Turn-off Delay Time	$t_{\text{D(off)}}$		-	19	-	
Turn-off fall Time	t_{f}		-	9	-	

- A. Repetitive rating; pulse width limited by max. junction temperature.
- B. $T_J=25^\circ\text{C}, V_G=10\text{V}, R_G=25\Omega, L=1\text{mH}, I_{AS}=12.5\text{A}$.
- C. P_d is based on max. junction temperature, using junction-case thermal resistance.
- D. The value of R_{GJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in the still air environment with $T_A=25^\circ\text{C}$. The maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.



■ Typical Electrical and Thermal Characteristics Diagrams

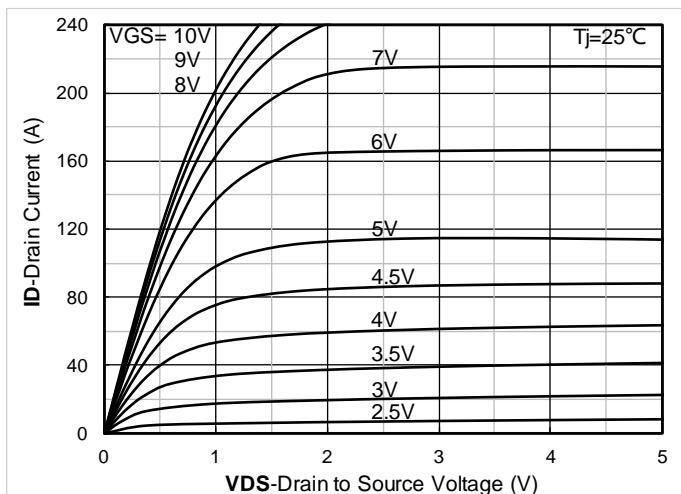


Figure 1. Output Characteristics

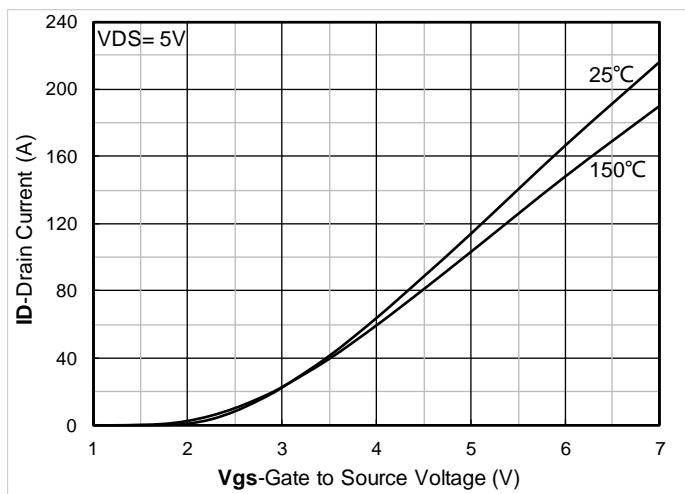


Figure 2. Transfer Characteristics

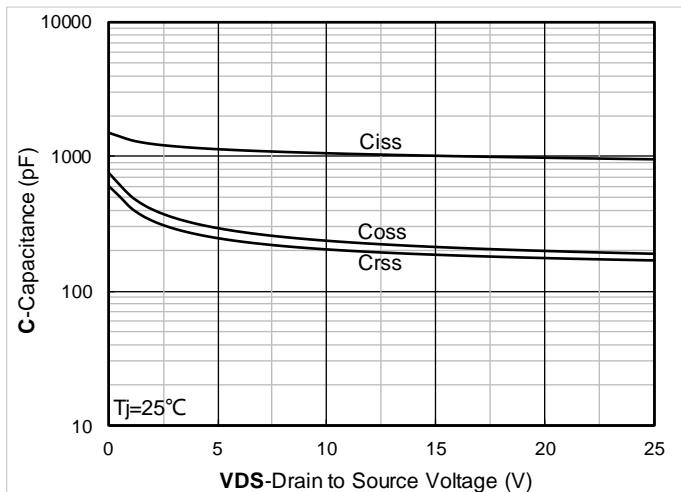


Figure 3. Capacitance Characteristics

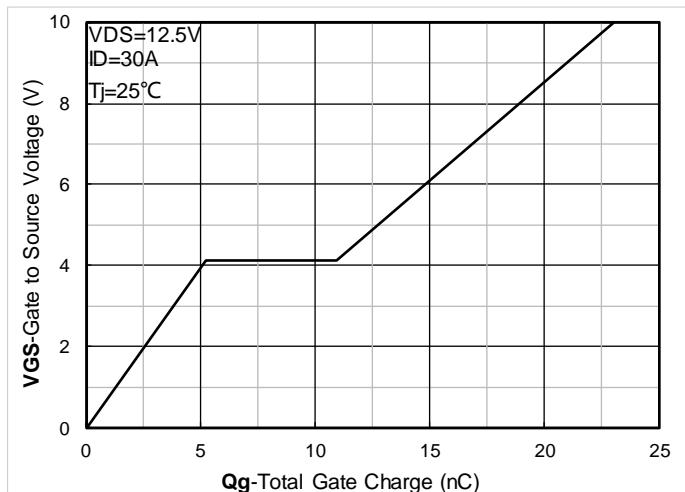


Figure 4. Gate Charge

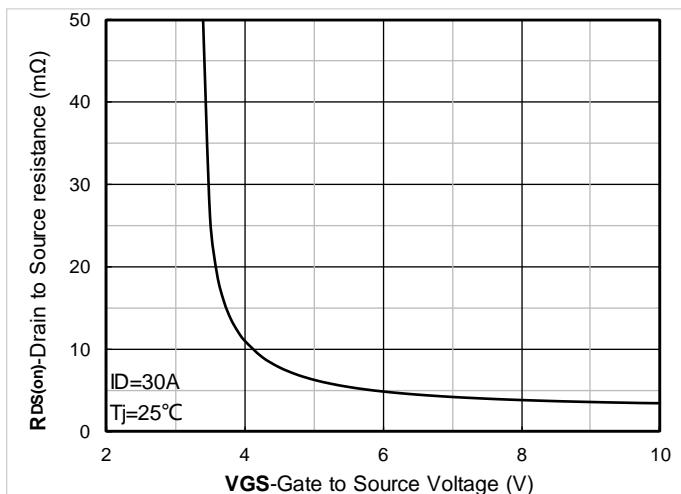


Figure 5. On-Resistance vs Gate to Source Voltage

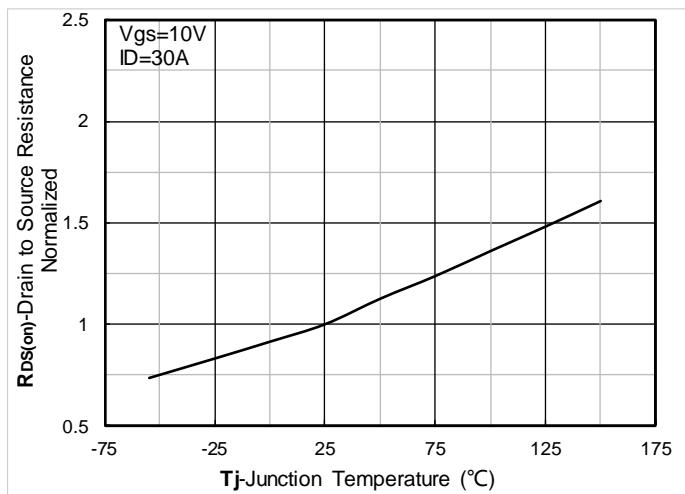


Figure 6. Normalized On-Resistance

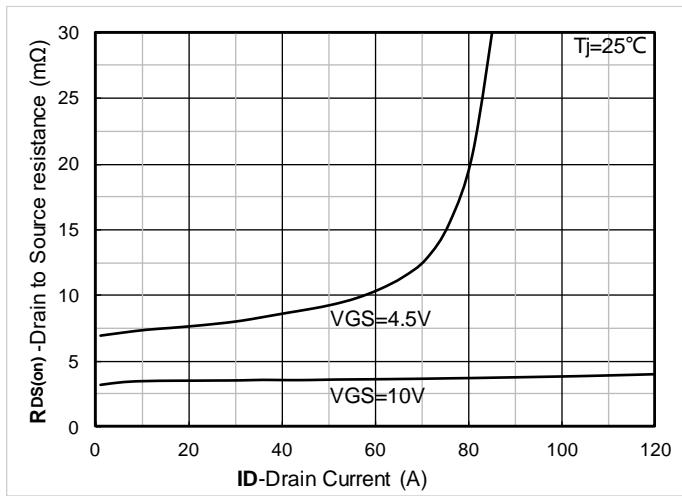


Figure 7. RDS(on) VS Drain Current

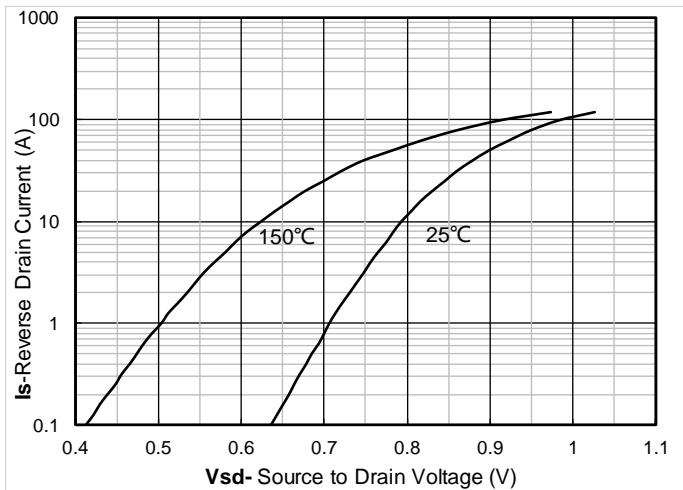


Figure 8. Forward characteristics of reverse diode

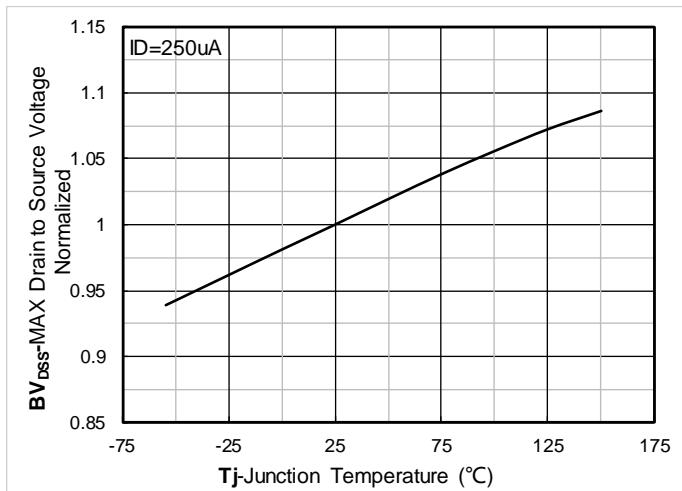


Figure 9. Normalized breakdown voltage

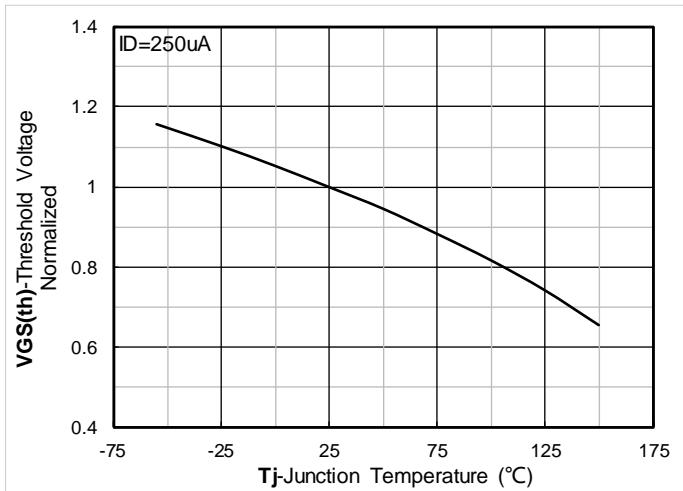


Figure 10. Normalized Threshold voltage

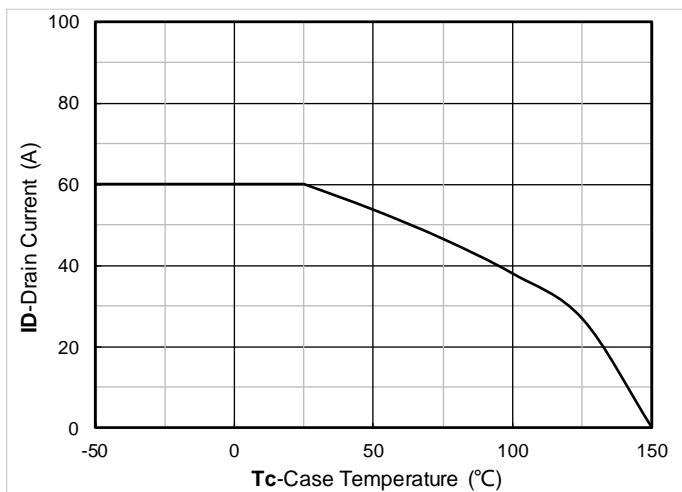


Figure 11. Current dissipation

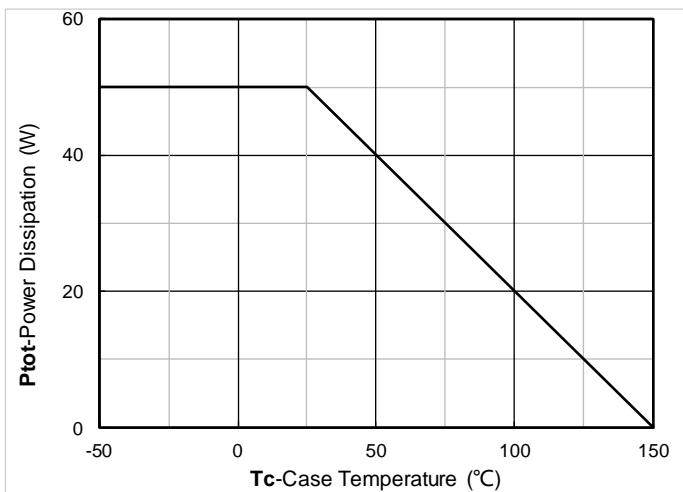


Figure 12. Power dissipation

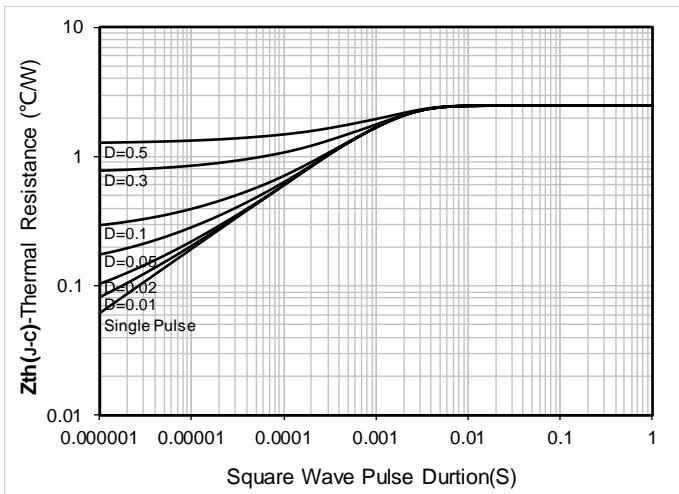


Figure 13. Maximum Transient Thermal Impedance

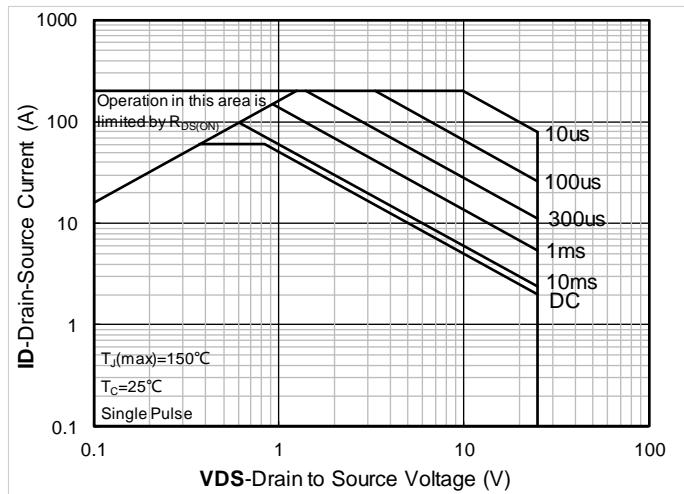


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

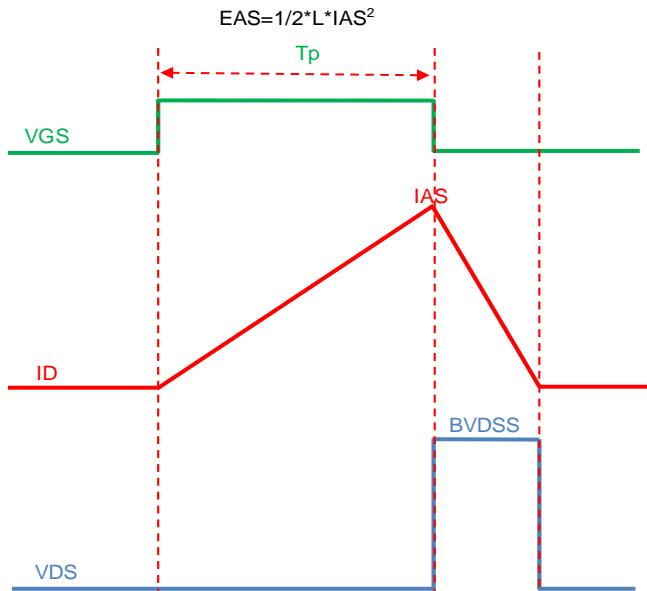
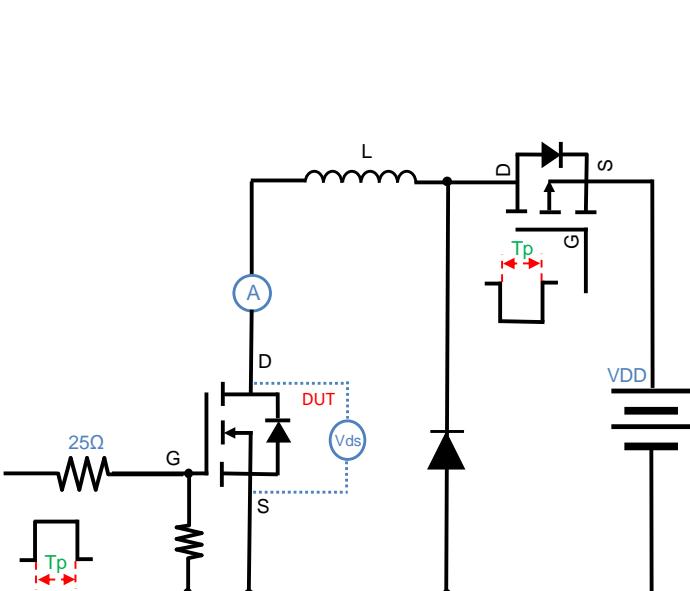


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

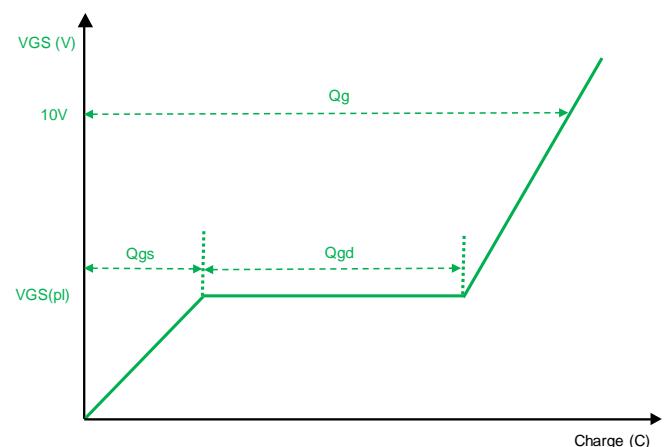
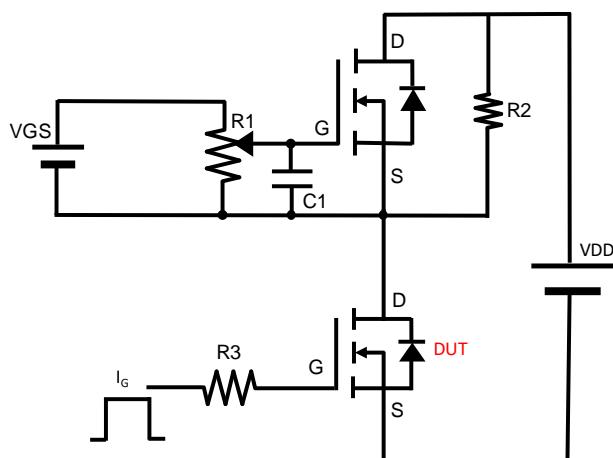


Figure B. Gate Charge Test Circuit & Waveform

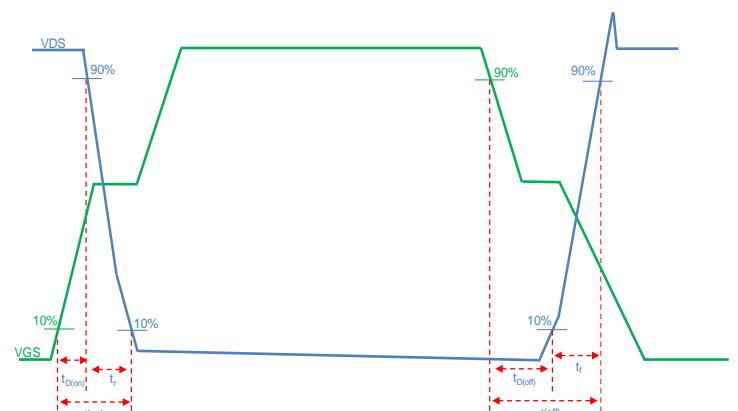
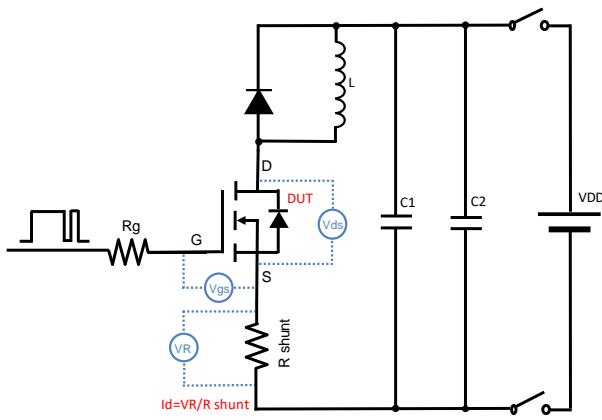


Figure C. Resistive Switching Test Circuit & Waveform

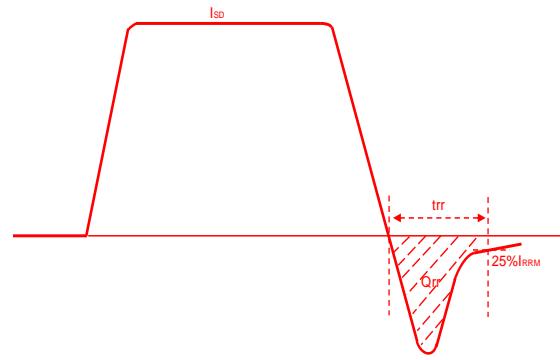
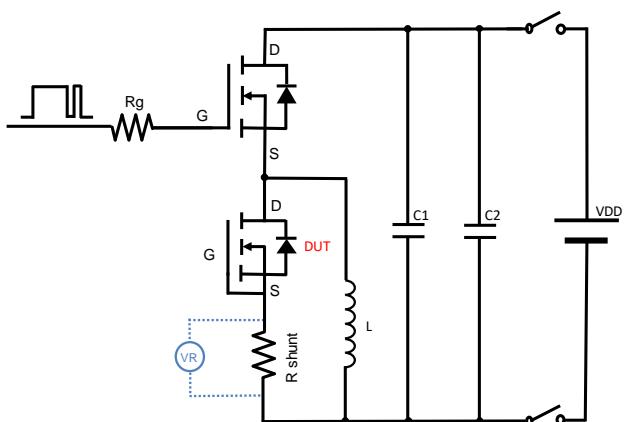
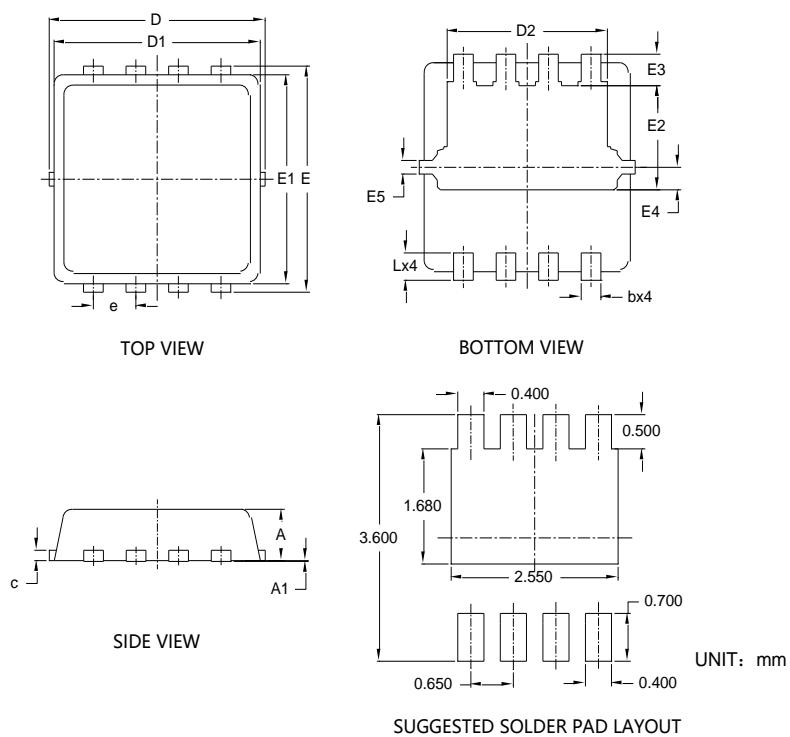


Figure D. Diode Recovery Test Circuit & Waveform



■ PDFN3333-8L-B Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.028	0.033	0.700	0.850
A1	0.000	0.002	0.000	0.050
b	0.008	0.016	0.200	0.400
c	0.004	0.010	0.100	0.250
D	0.124	0.136	3.150	3.450
D1	0.118	0.130	3.000	3.300
D2	0.089	0.104	2.250	2.650
E	0.124	0.136	3.150	3.450
E1	0.114	0.126	2.900	3.200
E2	0.052	0.068	1.320	1.720
E3	0.011	0.026	0.280	0.650
E4	0.013 REF		0.330 REF	
E5	0.008 REF		0.200 REF	
e	0.026 BSC		0.650 BSC	
L	0.012	0.020	0.300	0.500

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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